REMARKS

Claims 1 to 36 were pending in the application at the time of examination. The Examiner objected to FIG.s 1, 2, 3, and 6. The Examiner rejected Claims 1, 2, 4, 6, 7, 9 to 12, 14, 16, 17, 19 to 22, 24 26, 27 and 29 to 36 under 35 U.S.C. 102(b) as anticipated by the Mizuno et al. reference (US 6,229,360). The Examiner rejected Claims 3, 5, 13, 15, 18, 23, 25 and 28 under 35 U.S.C. 103(a) as obvious over the Mizuno et al. reference (US 6,229,360).

Applicant has amended FIG.s 1, 2, 3, and 6 in response to the Examiner's request. Applicant has amended Claims 1, 11, 21, 31, 32, 33, 34, 35, and 36. Applicant has canceled Claims 9, 19, 29 and 30, without prejudice

Consequently Claims 1 to 8, 11 to 18, 20 to 29, and 31 to 36 remain in the Application.

OBJECTION TO THE DRAWINGS

The Examiner objected to FIG.s 1, 2, 3, and 6. Filed herewith are four sheets of drawings including changes to FIG.1, FIG.2, FIG.3 and FIG.6. These sheets of drawings, which include FIG.1, FIG.2, FIG.3 and FIG.6, replaces the original sheets including FIG.1, FIG.2, FIG.3 and FIG.6.

In light of the replacements drawings filed herewith, Applicant respectfully requests the Examiner withdraw the objection to FIG.s 1, 2, 3 and 6.

REJECTION OF CLAIMS 1, 2, 4, 6, 7, 9 to 12, 14, 16, 17, 19 to 22, 24 26, 27 AND 29 to 36 UNDER 35 U.S.C. 102(b)

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Examiner rejected Claims 1, 2, 4, 6, 7, 9 to 12, 14, 16, 17, 19 to 22, 24 26, 27 and 29 to 36 under 35 U.S.C. 102(b) as anticipated by the Mizuno et al. reference (US 6,229,360).

Applicant has cancelled Claims 9, 19, 29 and 30, without prejudice. Consequently, Applicant respectfully submits that the rejection of Claims 9, 19, 29 and 30 is moot except to the extent these claims have been incorporated in the amendments discussed below.

Applicant has amended each of independent Claims 1, 11, 21, 31, 32, 33, 34, 35, and 36.

Claim 1, as amended, recites, with emphasis added:

> A clock skew tolerant clocking scheme comprising:
>
> a data stream;
>
> a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse rising edge and a clock pulse falling edge and a clock pulse width between said clock pulse rising edge and said clock pulse falling edge;
>
> a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse rising edge and a first pulse falling edge and a first pulse width between said first pulse rising edge and said first pulse falling edge, <u>said first pulse signal being generated by a first local pulse generator,</u> said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse rising edges of said first pulses are generated by a corresponding clock pulse rising edge of said corresponding one of

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said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse rising edge and a second pulse falling edge and a second pulse width between said second pulse rising edge and said second pulse falling edge, said second pulse signal being generated by a second local pulse generator, said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse rising edges of said second pulses are generated by a corresponding clock pulse falling edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

a first transparent pulse latch, said first pulse signal being operatively coupled to said first transparent pulse latch;

a second transparent pulse latch, said second pulse signal being operatively coupled to said second transparent pulse latch; wherein,

for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a rising edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a falling edge of said clock pulse; further wherein,

there is a frequency dependent separation window between a falling edge of said first pulse and rising edge of said corresponding second pulse such that race conditions are avoided.

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Claim 11, as amended, recites, with emphasis added:

A method for clocking combinational logic blocks said method comprising:

providing a data stream;

generating a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse rising edge and a clock pulse falling edge and a clock pulse width between said clock pulse rising edge and said clock pulse falling edge;

generating a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse rising edge and a first pulse falling edge and a first pulse width between said first pulse rising edge and said first pulse falling edge, **said first pulse signal being generated by a first local pulse generator,** said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse rising edges of said first pulses are generated by a corresponding clock pulse rising edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

generating a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse rising edge and a second pulse falling edge and a second pulse width between said second pulse rising edge and said second pulse falling edge, **said second pulse signal being generated by a second local pulse**

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generator, said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse rising edges of said second pulses are generated by a corresponding clock pulse falling edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

operatively coupling a first transparent pulse latch, to said first pulse signal;

operatively coupling a second transparent pulse latch to said second pulse signal;

ensuring that for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a rising edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a falling edge of said clock pulse; wherein, there is a frequency dependent separation window between a falling edge of said first pulse and rising edge of said corresponding second pulse such that race conditions are avoided.

Claim 21, as amended, recites, with emphasis added:

A method for creating a clock skew tolerate computer pipeline comprising;

providing a plurality of pipeline stages, each of said stages comprising combinational logic blocks, for each of said combinational logic blocks:

providing a data stream;

generating a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock

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pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse rising edge and a clock pulse falling edge and a clock pulse width between said clock pulse rising edge and said clock pulse falling edge;

generating a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse rising edge and a first pulse falling edge and a first pulse width between said first pulse rising edge and said first pulse falling edge, **said first pulse signal being generated by a first local pulse generator,** said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse rising edges of said first pulses are generated by a corresponding clock pulse rising edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

generating a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse rising edge and a second pulse falling edge and a second pulse width between said second pulse rising edge and said second pulse falling edge, **said second pulse signal being generated by a second local pulse generator,** said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse rising edges of said second pulses are generated by a corresponding clock pulse falling edge of said corresponding one of said plurality of clock pulses, said

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second pulse width being less than fifty percent of said clock pulse width;

operatively coupling a first transparent pulse latch, to said first pulse signal;

operatively coupling a second transparent pulse latch to said second pulse signal;

ensuring that for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a rising edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a falling edge of said clock pulse; wherein, there is a frequency dependent separation window between a falling edge of said first pulse and rising edge of said corresponding second pulse such that race conditions are avoided.

Claim 31, as amended, recites, with emphasis added:

A clock skew tolerant clocking scheme comprising:

a data stream;

a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse falling edge and a clock pulse rising edge and a clock pulse width between said clock pulse falling edge and said clock pulse rising edge;

a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse rising edge and a first pulse falling edge and a first pulse width between said first pulse rising edge and said first pulse falling edge, **said first**

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pulse signal being generated by a first local pulse generator, said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse rising edges of said first pulses are generated by a corresponding clock pulse falling edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse rising edge and a second pulse falling edge and a second pulse width between said second pulse rising edge and said second pulse falling edge, **said second pulse signal being generated by a second local pulse generator,** said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse rising edges of said second pulses are generated by a corresponding clock pulse rising edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

a first transparent pulse latch, said first pulse signal being operatively coupled to said first transparent pulse latch;

a second transparent pulse latch, said second pulse signal being operatively coupled to said second transparent pulse latch; wherein,

for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a falling edge of said clock pulse and a

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corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a rising edge of said clock pulse; further wherein,

there is a frequency dependent separation window between a falling edge of said first pulse and rising edge of said corresponding second pulse such that race conditions are avoided.

Claim 32, as amended, recites, with emphasis added:

A method for clocking combinational logic blocks said method comprising:

providing a data stream;

generating a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse falling edge and a clock pulse rising edge and a clock pulse width between said clock pulse falling edge and said clock pulse rising edge;

generating a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse rising edge and a first pulse falling edge and a first pulse width between said first pulse rising edge and said first pulse falling edge, **said first pulse signal being generated by a first local pulse generator,** said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse rising edges of said first pulses are generated by a corresponding clock pulse falling edge of said corresponding one of said plurality of clock pulses, said first pulse width being

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less than fifty percent of said clock pulse width;

generating a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse rising edge and a second pulse falling edge and a second pulse width between said second pulse rising edge and said second pulse falling edge, **said second pulse signal being generated by a second local pulse generator,** said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse rising edges of said second pulses are generated by a corresponding clock pulse rising edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

operatively coupling a first transparent pulse latch, to said first pulse signal;

operatively coupling a second transparent pulse latch to said second pulse signal;

ensuring that for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a falling edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a rising edge of said clock pulse; wherein,

there is a frequency dependent separation window between a falling edge of said first pulse and rising edge of said corresponding second pulse such that race conditions are avoided.

Claim 33, as amended, recites, with emphasis added:

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A method for creating a clock skew tolerate computer pipeline comprising;

providing a plurality of pipeline stages, each of said stages comprising combinational logic blocks, for each of said combinational logic blocks:

providing a data stream;

generating a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse falling edge and a clock pulse rising edge and a clock pulse width between said clock pulse falling edge and said clock pulse rising edge;

generating a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse rising edge and a first pulse falling edge and a first pulse width between said first pulse rising edge and said first pulse falling edge, **said first pulse signal being generated by a first local pulse generator,** said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse rising edges of said first pulses are generated by a corresponding clock pulse falling edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

generating a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse rising edge and a second pulse falling edge and a second pulse width between said second pulse rising edge and said second pulse falling

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edge, **said second pulse signal being generated by a second local pulse generator,** said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse rising edges of said second pulses are generated by a corresponding clock pulse rising edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

operatively coupling a first transparent pulse latch, to said first pulse signal;

operatively coupling a second transparent pulse latch to said second pulse signal;

ensuring that for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a falling edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a rising edge of said clock pulse; wherein,

there is a frequency dependent separation window between a falling edge of said first pulse and rising edge of said corresponding second pulse such that race conditions are avoided.

Claim 34, as amended, recites, with emphasis added:

A clock skew tolerant clocking scheme comprising:

a data stream;

a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality

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of clock pulses comprising a clock pulse first edge and a clock pulse second edge and a clock pulse width between said clock pulse first edge and said clock pulse second edge;

a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse first edge and a first pulse second edge and a first pulse width between said first pulse first edge and said first pulse second edge, **said first pulse signal being generated by a first local pulse generator,** said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse first edges of said first pulses are generated by a corresponding clock pulse first edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse first edge and a second pulse second edge and a second pulse width between said second pulse first edge and said second pulse second edge, **said second pulse signal being generated by a second local pulse generator,** said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse first edges of said second pulses are generated by a corresponding clock pulse second edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

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a first transparent pulse latch, said first pulse signal being operatively coupled to said first transparent pulse latch;

a second transparent pulse latch, said second pulse signal being operatively coupled to said second transparent pulse latch; wherein,

for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a first edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a second edge of said clock pulse; further wherein,

there is a frequency dependent separation window between a second edge of said first pulse and first edge of said corresponding second pulse such that race conditions are avoided.

Claim 35, as amended, recites, with emphasis added:

A method for clocking combinational logic blocks said method comprising:

providing a data stream;

generating a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse first edge and a clock pulse second edge and a clock pulse width between said clock pulse first edge and said clock pulse second edge;

generating a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse first edge and a first pulse second edge and a first pulse width between said first pulse first edge

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and said first pulse second edge, **said first pulse signal being generated by a first local pulse generator,** said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse first edges of said first pulses are generated by a corresponding clock pulse first edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

generating a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse first edge and a second pulse second edge and a second pulse width between said second pulse first edge and said second pulse second edge, **said second pulse signal being generated by a second local pulse generator,** said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse first edges of said second pulses are generated by a corresponding clock pulse second edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

operatively coupling a first transparent pulse latch, to said first pulse signal;

operatively coupling a second transparent pulse latch to said second pulse signal;

ensuring that for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a first edge of

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said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a second edge of said clock pulse; wherein,

there is a frequency dependent separation window between a second edge of said first pulse and first edge of said corresponding second such that race conditions are avoided.

Claim 36, as amended, recites, with emphasis added:

A method for creating a clock skew tolerate computer pipeline comprising;

providing a plurality of pipeline stages, each of said stages comprising combinational logic blocks, for each of said combinational logic blocks:

providing a data stream;

generating a clock signal, said clock signal having a clock cycle, said clock signal comprising a plurality of clock pulses, each of said clock pulses of said plurality of clock pulses comprising a clock pulse first edge and a clock pulse second edge and a clock pulse width between said clock pulse first edge and said clock pulse second edge;

generating a first pulse signal, said first pulse signal comprising a plurality of first pulses, each of said first pulses of said plurality of first pulses comprising a first pulse first edge and a first pulse second edge and a first pulse width between said first pulse first edge and said first pulse second edge, **said first pulse signal being generated by a first local pulse generator,** said first pulse signal being derived from said clock signal such that each of said first pulses of said plurality of first pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said first pulse first edges of said first

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pulses are generated by a corresponding clock pulse first edge of said corresponding one of said plurality of clock pulses, said first pulse width being less than fifty percent of said clock pulse width;

generating a second pulse signal, said second pulse signal comprising a plurality of second pulses, each of said second pulses of said plurality of second pulses comprising a second pulse first edge and a second pulse second edge and a second pulse width between said second pulse first edge and said second pulse second edge, **said second pulse signal being generated by a second local pulse generator,** said second pulse signal being derived from said clock signal such that each of said second pulses of said plurality of second pulses corresponds to one of said clock pulses of said plurality of clock pulses and each of said second pulse first edges of said second pulses are generated by a corresponding clock pulse second edge of said corresponding one of said plurality of clock pulses, said second pulse width being less than fifty percent of said clock pulse width;

operatively coupling a first transparent pulse latch, to said first pulse signal;

operatively coupling a second transparent pulse latch to said second pulse signal;

ensuring that for each clock pulse of said plurality of clock pulses of said clock signal there is a first pulse of said plurality of first pulses of said first pulse signal generated by a first edge of said clock pulse and a corresponding second pulse of said plurality of second pulses of said second pulse signal generated by a second edge of said clock pulse; wherein, there is a frequency dependent separation window between a second edge of said first pulse and first edge of said corresponding second such that race conditions are avoided.

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As shown above, each of Applicants independent Claims 1, 11, 21, 31, 32, 33, 34, 35 and 36, as amended now includes the limitation of "said first pulse signal being generated by a first local pulse generator" and "said second pulse signal being generated by a second local pulse generator"

These amendment are supported by: Applicant' FIG. 6 as filed; Applicants Claims 9, 10, 19, 20, 29 and 30 as filed; and Applicant's Specification as filed. For instance, Applicant's Specification at page 20, line 24 to page 21, line 25, reads as follows with emphasis added:

> FIG. 6 shows one embodiment of dual transparent pulsed latches (601 and 603) operated by complementary phases of the clock signal in accordance with one embodiment of the invention. As shown in FIG.6, in one embodiment of the invention, a first pulse latch 601 includes a first **pulse generator 602 for producing a first pulse, such as first pulses 411, 413 and 415 in FIG.4 and 511, 513 and 515 in FIG.5, derived from the rising edge of a clock pulse. Also shown in FIG. 6 is a second pulse latch 603 including a second pulse generator 604 for producing a second pulse, such as second pulses 421, 423 and 425 in FIG.4 and 521, 523 and 525 in FIG.5, derived from the trailing edge of a clock pulse. Logic block 611 is coupled between pulse latches 601 and 603.** Likewise, logic block 613 is coupled between second pulse latch 603 and third pulse latch 605. **According to one embodiment of the invention, third pulse latch 605, like first pulse latch 601, includes a first pulse**

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generator 606 for producing a first pulse, such as first pulses 411, 413 and 415 in FIG.4 and 511, 513 and 515 in FIG.5, derived from the rising edge of a clock pulse.

Pulse latches and their operation are well known to those of skill in the art. Consequently, the structure and methods of pulse latches is not discussed in more detail herein to avoid detracting from the present invention. For a more detailed discussion of pulse latches the reader is referred to virtually any computer engineering text book. For example, "THE COMPUTER ENGINEERING HANDBOOK", edited by Vojin G. Oklobdzija, CRC press 2002, ISBN 0-8493-0885-1, see chapter 10.2 "LATCHES AND FLIP-FLOPS", authored by the present inventor, pages 10-35 to 10-52.

As shown in FIG.6, in one embodiment of the invention, the first and second pulses are generated locally by pulse generators 602, 604 and 606 and therefore, in one embodiment of the invention, the system remains a single-phase system and there is no need to distribute additional signals widely.

In contrast to the method and structure discussed above, and recited in Applicant's Claims 1, 11, 21, 31, 32, 33, 34, 35 and 36, as amended, the Mizuno et al. reference specifically states that the disclosed system relies on a commonly supplied clock signal and fails to disclose or discuss local pulse generators at all (see the Mizuno et al. reference abstract, FIG.1 and clock tree 6, and FIG.s 2, 3, and 4 cited by the Examiner). Therefore, applicant respectfully submits that the Mizuno et al. reference not only fails to disclose, teach or

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suggest "said first pulse signal being generated by a first local pulse generator" and "said second pulse signal being generated by a second local pulse generator" as recited in Applicant's Claims 1, 11, 21, 31, 32, 33, 34, 35 and 36, as amended, but the Mizuno et al. reference actually teaches away from this feature.

In light of the discussion above, Applicant respectfully submits that the Mizuno et al. reference neither discloses, teaches nor suggests Applicant's invention as recited in independent Claims 1, 11, 21, 31, 32, 33, 34, 35 and 36, as amended, and that Claims 1, 11, 21, 31, 32, 33, 34, 35 and 36, as amended, are therefore patentable over the Mizuno et al. reference. Consequently, Applicant respectfully requests the Examiner withdraw the rejection of Claims 1, 11, 21, 31, 32, 33, 34, 35 and 36, as amended, under 35 U.S.C. 102(b) and allow Claims 1, 11, 21, 31, 32, 33, 34, 35 and 36, as amended, to issue.

In addition, Claims 2, 4, 6, 7, and 10 depend, directly or indirectly, on Claim 1, as amended, consequently Claims 2, 4, 6, 7, and 10 include all of the features and limitations of Claim 1, as amended, and are therefore patentable over the Mizuno et al. reference for at least the reasons discussed above. Consequently Applicant respectfully requests the Examiner withdraw the rejection of Claims 2, 4, 6, 7, and 10 under 35 U.S.C. 102(b) and Allow Claims 2, 4, 6, 7, and 10 to issue.

In addition, Claims 12, 14, 16, 17, and 20 depend, directly or indirectly on Claim 11, as amended, consequently Claims 12, 14, 16, 17, and 20 include all of the features and limitations of Claim 11, as amended, and are therefore patentable over the Mizuno et al. reference for at least the reasons discussed above. Consequently Applicant respectfully requests the Examiner withdraw the rejection of Claims 12, 14,

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16, 17, and 20 under 35 U.S.C. 102(b) and allow Claims 12, 14, 16, 17, and 20.

In addition, Claims 22, 24 26, and 27 depend, directly or indirectly on Claim 21, as amended, consequently Claims 22, 24 26 and 27 include all of the features and limitations of Claim 21, as amended, and are therefore patentable over the Mizuno et al. reference for at least the reasons discussed above. Consequently Applicant respectfully requests the Examiner withdraw the rejection of Claims 22, 24 26 and 27 under 35 U.S.C. 102(b) and allow Claims 22, 24 26, and 27 to issue.

REJECTION OF CLAIMS 3, 5, 13, 15, 18, 23, 25 AND 28 UNDER 35 U.S.C. 103(a)

The Examiner rejected Claims 3, 5, 13, 15, 18, 23, 25 and 28 under 35 U.S.C. 103(a) as obvious over the Mizuno et al. reference (US 6,229,360).

For the at least reasons discussed in more detail above, Applicant respectfully submits that the Mizuno et al. reference neither discloses, teaches nor suggests Applicant's invention as recited in independent Claims 1, 11, 21, 31, 32, 33, 34, 35 and 36, as amended, and therefore, Applicant respectfully submits that Claims 1, 11, 21, 31, 32, 33, 34, 35 and 36, as amended, are patentable over the Mizuno et al. reference under either 35 U.S.C. 102(b) or 35 U.S.C. 103(a).

Claims 3, 5 and 8 depend, directly or indirectly, on Claim 1, as amended, consequently Claims 3, 5 and 8 include all of the features and limitations of Claim 1, as amended, and are therefore patentable over the Mizuno et al. reference for at least the reasons discussed above. Consequently Applicant respectfully requests the Examiner withdraw the rejection of Claims 3 and 5 under 35 U.S.C. 103(a) and allow Claims 3 and 5 to issue.

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In addition, Claims 13, 15, and 18 depend, directly or indirectly on Claim 11, as amended, consequently Claims 13, 15, and 18 include all of the features and limitations of Claim 11, as amended, and are therefore patentable over the Mizuno et al. reference for at least the reasons discussed above. Consequently Applicant respectfully requests the Examiner withdraw the rejection of Claims 13, 15, and 18 under 35 U.S.C. 103(a) and allow Claims 13, 15, and 18 to issue.

In addition, Claims 23, 25 and 28 depend, directly or indirectly on Claim 21, as amended, consequently Claims 23, 25 and 28 include all of the features and limitations of Claim 21, as amended, and are therefore patentable over the Mizuno et al. reference for at least the reasons discussed above. Consequently Applicant respectfully requests the Examiner withdraw the rejection of Claims 23, 25 and 28 under 35 U.S.C. 103(a) and allow Claims 23, 25 and 28 to issue.

CONCLUSION

For the foregoing reasons, Applicant respectfully requests allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on December 20, 2004.

Attorney for Applicant — December 20, 2004 Date of Signature

Respectfully submitted,

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Amendments to the Drawings:

The attached sheets of drawings includes changes to FIG.1, FIG.2, FIG.3 and FIG.6. These sheets of drawings, which include FIG.1, FIG.2, FIG.3 and FIG.6, replaces the original sheets including FIG.1, FIG.2, FIG.3 and FIG.6.

Attachment: Replacement Sheets for FIG.1, FIG.2, FIG.3 and FIG.6

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